Implementation of a novel buck-boost converter based on coupled inductor for renewable energy applications

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ORIGINAL PAPER

Implementation of a novel buck-boost converter based on coupled inductor for renewable energy applications

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A coupled inductor based on dual switches buck-boost converter is proposed in the article, which can be used in renewable energy applications. Wide conversion ratio can be realized by regulating turns ratio of the coupled inductor and the duty cycle. The topology has a quadratic- like voltage gain, and the low voltage stress and current stress. Combing the passive clamping circuit to recover leakage energy, the voltage spikes of power switches are suppressed, improving the efficiency. Moreover, it has the merits of continuous input current and common ground. To demonstrate the superior performances of the presented converter, the principle of operation and steady-state analysis are presented in detail. At last, a 100 W experimental prototype was designed to verify the correctness of the theoretical analysis, with a maximum efficiency of 95.7% in step-up mode and 96.8 % in step-down mode.

KEYWORDS

Buck-boost converter, coupled inductor, renewable energy

INTRODUCTION

Due to the scarcity of the improvement of environmental awareness and fossil fuel energy, the renewable energy has drawn more attention[1,2]. Photovoltaic (PV) and wind power play a crucial role in industrial applications, reducing the pollution[3]. However, climate and weather patterns can cause renewable energy sources to produce inconsistent and intermittent output voltage [4]. Buck-boost converter can regulate the voltage, which is suitable for renewable energy conversion[5].

The typical buck-boost converter can achieve wide range of input voltage with simple structure, which has been researched in recent years[6,7]. However, its applications are limited by voltage gain and non-common ground[8,9]. To achieve these issues, the CUK, ZETA and SEPIC converter basic on buck-boost converter are proposed. However, the semiconductors are withstand high voltage stress and current stress [10].

To improve the above shortcomings, some transformerless single switch buck-boost converters are proposed. In Banaei and Bonab[11], a ZETA converter based buck-boost circuit is presented to achieve higher voltage gain than traditional buck-boost converter. However, the improvement of voltage gain is limited. Converters in Gorji, et al.[12] and Shu, et al.[13] propose the quadratic voltage gain buck-boost converter that effectively increase the voltage with the narrow range of duty cycle. But the above quadratic buck-boost converters have disadvantage of high input current ripple. To achieve continuous input current and decrease the input ripple, the inductor is joined straightforwardly to the input source.[14,15]. Combing the quadratic cell and continues input current technology, converter in Zhang, et al.[16] and Kumar and Krishnasamy[17] are proposed to obtain high voltage gain only by adjusting the duty cycle. Coupled inductor is another technology which has been used widely in converter to improve the voltage gain by regulating the turns ratio. Considering the leakage inductor of coupled inductor, the passive clamp circuit can be employed to recycle the energy of leakage inductor and suppress the voltage spike of power switch[18,19]. Rong, et al.[20]proposes a passive clamp circuit-based buck-boost-Cuk converter that employs a coupled inductor to achieve higher voltage gain. But it is a non-common ground structure which increases the difficulty of control system and electromagnetic interference (EMI). In Alizadeh, et al.[21], a single switch quadratic buck-boost converter based on coupled inductor is presented, which has the benefits of common ground and continuous input current. Also, it has the disadvantage that the voltage stress of the power switch is high.

To decrease the voltage stress and current stress on the semiconductor, dual switches structure is widely utilizing in power electronics converter[22,23]. Some dual switches buck-boost converters are proposed in the recent time. Combing continuous input and quadratic, a dual switches converter is proposed[24]. To further decrease the voltage stress of the power switches, a family of cascading of boost and ZETA structure converters are proposed in Veerachary and Khuntia[25]. Compared with the above relevant dual switches converter, converter in Okati, et al.[26] has higher conversion ratio. To solve the effect of non-common and hold on the voltage gain with previous converter, a modified SEPIC converter is proposed in Wang, et al.[27]. A novel negative output buck-boost converter in Ding and Wang[28] and a converter with interleaving two CUK converters in Taghizadegan Kalantari, et al.[29] are proposed, which achieve wider conversion ratio than above dual switches converter and have non-common ground structure. Converter in Hosseinpour, et al.[30] proposes a dual switches converter with common ground structure. The circuit achieves high voltage gain while minimizing the voltage stress of the switch through increment passive components' number, which make the converter bulky.

Considering the above technology, this article proposes a dual switches buck-boost converter based on coupled inductor. Applying coupled inductor, high voltage gain can be attained by regulating both the duty cycle and the turns ratio. The quadratic- like voltage gain is achieved to wide conversion ratio. Moreover, the voltage stress and current stress are lower than traditional quadratic cell. The passive clamp circuit effectively suppresses voltage spike of the power switches, also recycling the energy of leakage inductor. Common ground between input sources and load reduces the EMI and difficulty of the control design. Therefore, the proposed converter can attain output voltage with stability and suitability for solving the issues of renewable energy applications.

In this paper, Section 2 analyzes the operation principles. The stead-state analysis, which includes the voltage gain and stresses of components, is discussed in Section 3. The component parameter design and power loss analysis for the proposed converter are discussed in Section 4 and Section 5, respectively. Section 6 is a comparison of the characteristics of the relevant converters which can demonstrate the superior of the presented converter. Section 7 demonstrates the experiment results with open loop and close loop in both step-up and step-down modes.

OPERATION PRINCIPLES

The equivalent circuit of dual switches coupled inductor buck-boost converter is given in Fig. 1, which is assembled from two power switches S_1 andS_2, three capacitors C_1,C_2, and C_o , three diodesD_1, D_2 andD_3, an inductor L_1, and a coupled inductor. Coupled inductor combines with leakage inductorL_k , magnetizing inductorL_m and ideal transformer with primary windingL_p and secondary windingL_s . Two power switches operate synchronously. To simplify the calculation of steady-state analysis, several assumptions are considered as follow:

1. The values of capacitors are large enough so that the voltage of each capacitor is regarded as constant in a switching cycle.
2. The parasitic resistance and forward voltage drop of the components can be ignored.
3. The turns ratio of coupled inductor can be defined as$N_p : N_s = 1 :$ n.
4. The coupling coefficient k is defined as L_m / (L_m + L_k).

Fig. Equivalent circuit.

Fig. 2 shows the voltage and current waveforms with main components of the converter which operates in continuous conduction mode (CCM). Current flow paths of three operating modes in a switching cycle are plotted in Fig. 3.

Mode I (t_0-t_1) [Fig. 3(a)]: The power switches S_1 andS_2 are turned on; diodesD_1 and D_3 are reverse biased, diode D_2 is on. The magnetizing inductorL_m is charged by V_{in} , and capacitors C_1 and C_2release energy to inductor L_1.C_o provides energy to the load.i_{L1} starts to increase andi_{Lk} increases rapidly. This mode ends whileD_2 is off.

Mode II (t_1-t_2) [Fig. 3(b)]: The power switches S_1 andS_2 are still remain activated while all diodes are reverse biased. Other current flow paths are same as Mode I. Besides, the currents of L_m andL_1 increase. i_{Lm} starts to increase. When the signal of power switches becomes low, this mode ends. Some equations can be obtained in this mode as following.

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Mode III (t_2-t_3) [Fig. 3(c)]: The power switches S_1 andS_2 are turned off simultaneously. DiodesD_1, D_2, andD_3 are forward biased. CapacitorC_1 is charged by the magnetizing inductorL_m and V_{in} . Meanwhile, the magnetizing inductor L_m transfers energy to the secondary side of coupled inductor. Capacitor C_2stores the energy through the coupled inductor andD_2. The inductor L_1releases energy to the output capacitor C_o and the load through D_3. The current values ofL_k , L_m andL_1 are above zero and decrease. When the signal of power switches becomes high, this mode ends. Some equations can be obtained in this mode as follows:

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(a) (b)

Fig. The key waveforms of the main components under (a) step-up mode; (b) step-down mode.

(a)

(b)

(c)

Fig. . The operating modes (a) Mode I, (b) Mode II, (c) Mode III.

STEADY-STATE ANALYSIS

Voltage Gain

Utilizing (2) and (6), by applying the principle of voltage-second balance on the magnetizing inductor Lm , (10) can be deduced as following.

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The voltage across C_1 can be given.

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Using (6) and (11), the voltage stress of C_2 can be obtained.

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From (1) and (5), by applying the principle of voltage-second balance onL_1, the voltage gain M can be achieved as

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Substituting (11) and (12) into (13), the voltage gain M can be achieved.

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The correlation among voltage gain M , duty cycle D , and coupling coefficient k under n =1 is illustrated in Fig. 4. The coupling coefficient has almost no impacts to the voltage gain. Hence the coupling coefficient can be setting as k =1. The ideal voltage gain can be calculated in (15).

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Fig. . The correlation among voltage gain M , duty cycle D , and coupling coefficient$k$.

Semiconductors' Voltage Stresses

When power switches are turned on, using Kirchhoff's Voltage Law (KVL), from (1), (11), and (12), the voltage stresses of diodes are derived as

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From Fig. 3 (c), (11), (12), and (15), the voltage stresses of power switches are expressed as

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Semiconductors' Current Stresses

During a switching cycle, applying the Kirchhoff's Current Law (KCL), the currents of the capacitors C_o andC_1 can be written.

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By applying the principle of ampere-second balance capacitorC_o , the average current of the inductorL_1 can be achieved as (23).

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Similarly, based on (22), the average current acrossD_1 in conducting time is presented as

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From (24), during a switching cycle, we can derive the average current of D_1 as

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From Fig. 1 and (23), according to KCL and the principle of ampere-second balance, the following average currents ofD_3 and D_2 can be given, respectively.

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Similarly, using (15) and (27), the average currents flowing through the power switches S_1 and S_2can be written as follows:

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Applying (27) and (28), the average current flowing through the magnetizing inductor L_m is given similarly

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Calculating the current ripples of inductors $L_1$and L_m can be achieved as (31) and (32), respectively.

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According to (23), (30)-(32), the maximum and minimum currents ofL_1 and L_m are achieved.

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According to KCL, the currents of diodes D_1,D_2 and D_3 during a switching cycle can be written as follows:

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Utilizing (37)-(39), the root-mean-square (RMS) currents of the diodes can be derived.

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Within one switching cycle, the expressions of the leakage inductor current i_{Lk} and the secondary winding currenti_{Ls} through the coupling inductor are as follows, respectively.

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According to the (23), (43) and (44), the RMS currents of the magnetics components can be derived.

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In a switching cycle, the currents of capacitorsC_1, C_2 andC_o can be derived applying KCL.

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From (48)-(50), the RMS currents flowing through the capacitors are expressed as

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During a switching cycle, according to KCL, the currents of the power switches can be derived as.

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From the equations (54) and (55), the RMS currents flowing through the power switches can be deduced.

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Due to the power switches are on during Mode II, the peak currents flowing through the power switches can be presented as

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For the power switches, the current expressions for these two instantaneous moments can be derived.

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COMPONENT PARAMETER DESIGN

Design of Inductors

Assuming that I_{oB} is the output current of boundary conduction mode (BCM). The average currents flowing throughL_1 and L_m in BCM are equal to half of the current ripple of L_1 andL_m , respectively.

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According to (62) and (63), the values of inductorsL_1 and L_m can be deduced.

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Design of Capacitors

Considering the voltage ripples of capacitors, the values of capacitor are designed suitable to increase the efficiency and stability. The voltage ripples Δv_{C1} , $\Delta v_{C2}$and Δv_{Co} can be derived as follows:

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POWER LOSS ANALYSIS

To analyze the presented converter efficiency, the power loss is divided into four parts, including inductors loss, power switches loss, diodes loss, capacitors loss. The parasitic parameters are defined as follows:r_{L1}, r_{Lp} , and r_{Ls} are the equivalent series resistance (ESR) of the inductor L_1 and the windingL_p and L_s , respectively;$P_{cv,L1}$ and$P_{cv,cp}$ are the core losses per unit volume, and $V_{e,L1}$ and $V_{e,cp}$ are the core volumes of inductorL_1 and coupled-inductor, respectively;r_{ds} is the power switch's on-resistance;t_{on} is the summary of rise time and delay time and t_{off} is the summary of fall time and delay time; V_{Dx} and r_{Dx} are the diodes forward drop voltage and forward resistance of diodesD_x (x =1, 2, 3),respectively; r_{Ci} is the ESR of the capacitorsC_i (i = 1, 2, o). The power loss analysis in detail will be expressed as following.

Power Loss of Inductors

Inductors power loss is divided into winding loss and core loss. The winding loss relies on the flowing current and ESR of winding, which can be derived as

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The core losses of inductor L_1 and coupled inductor can be calculated as

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From (69) and (70), the total loss of the inductors can be expressed as

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Power Loss of Power Switches

The power loss of power switches includes the conduction loss caused by on-resistance, and the switching loss caused by the transition times when the power switches are turning on and turning off.

The power switches' conduction and switching losses of the power switches can be calculated as (72) and (73).

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Therefore, (74) gives the total loss of S_1 and S_2.

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Power Loss of Diodes

The power loss of the diodes is mainly caused by the forward voltage drops and resistance of diodes, which can be derive as

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Therefore, the power loss of the diodes can be calculated as follows

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Power Loss of Capacitors

Due to the power loss of capacitors is caused by the ESR of capacitor, the power loss of the capacitors can be expressed.

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Efficiency Calculation

The total losses can be calculated as

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The efficiency calculation of the proposed converter can be calculated as following.

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COMPARISON

Comparing performance between the proposed converter and relevant converters is provided in Table 1. Fig. 5 (a) and (b) show the comparison results under n =1 with voltage gain in both step-up and step-down modes, respectively. Fig. 6 (a) and (b) give voltage stress on power switch, and current stress on power switch, respectively.

In step-up mode, the proposed converter has higher voltage gain than converter in Banaei and Ajdar Faeghi Bonab[14], Sarikhani, et al.[24] , and Wang, et al.[27]. In step-down mode, converters in Banaei and Ajdar Faeghi Bonab[14], Dhimish and Schofield[15], Kumar and Krishnasamy[17], and Hosseinpour, et al.[30] of voltage gain are less than proposed converter. Although the voltage gain in Alizadeh, et al.[21] is equal to the proposed converter, the current stress of power switch in this converter is considerably larger than the proposed converter. In the operating condition of experiment, the voltage stress of power switch has the superior performance comparing with the relevant converters except for the power switch$S$ $_2$ of the converter in Wang, et al.[27]. Additionally, the current stresses of power switches S $_1$ and S $_2$ in Wang, et al.[27] are higher than the current stresses of$S$ $_1$ and S $_2$ in the proposed converter, respectively. Moreover, the proposed converter has lower number of inductors and higher frequency than relevant converters to decrease the volume of the converter.

Table Comparing performance between the proposed converter and relevant converters.

Topology	Converter in Banaei and Ajdar Faeghi Bonab[14]	Converter in Dhimish and Schof
S	1	1
L	3	2
C	4	6
D	2	4
Number of Components	10	13
C.G	Yes	Yes
Voltage Gain (M)		
Voltage Stress of Switch S_1 (V_{ds1}/V_{in})		
Voltage Stress of Switch S_2 (V_{ds2}/V_{in})	-	-
Current Stress of Switch S_1 (I_{ds1}/I_o)		
Current Stress of Switch S_2 (I_{ds2}/I_o)	-	-
Frequency	40 kHz	75 kHz

S = Switch, D = Diode, C = Capacitor, C.G = Common ground between input sources and load.

(a) (b)

Fig. Comparison results of voltage gain in (a) step-up and step-down mode; (b) step-down mode.

(a) (b)

Fig. 6 Comparison of power switches on (a) voltage stress; (b) current stress.

EXPERIMENTAL RESULTS

To verify and test the presented converter, Table 2 demonstrates the experimental parameters.

From (15), the curves of voltage gain versus duty cycle in various turns ratio are plotted in Fig. 7. Considering the converter operate in the step-up mode and step-down mode with suitable duty cycle, the turns ratio n is selected as 1.

The experiment waveforms under step-up mode under$V_{in} = 15$ V, $V_o = 48$ V, and$P_o = 100$ W are illustrated in Fig. 8. Fig. 8 (a) and (b) show the voltage stresses of power switches (V_{ds} $_1$ andV_{ds} $_2$) which are 31 V and 62 V, respectively, verifying (19) and (20). The voltage spike of power switches can be inhibited by clamp circuit. The current waveform of inductor L $_1$ matches the expected behavior based on theoretical analysis. Fig. 8 (c), (d) and (e) show the voltage waveforms and current waveforms of the diodes D $_1$,D $_2$, and D $_3$, respectively. The voltage stresses of V_D $_1$,V_D $_2$, andV_D $_3$ are about 30V, 30V, and 94V, respectively. Therefore, the (16), (17) and (18) are evidenced. The current of D $_2$ achieves ZCS when$D$ $_2$ is turned off. At the same time, the leakage inductor on the secondary side of the coupled inductor is resonant with the parasitic capacitor of D $_2$. Thus, the voltage of diode D $_2$ have resonance phenomena, affecting the current and voltage of L_k .L_k resonates with the parasitic capacitors of the diodes and power switches during diodes are turn-on, resulting in the resonance of the voltages and currents of the semiconductor.

The waveforms of experiment under step-down mode under $V_{in} = 75$ V, $V_o = 48$ V, and $P_o = 100$ W are shown in Fig. 9. Fig. 9 (a) and (b) show the voltage stresses of power switches ($V_{ds\ 1}$ and $V_{ds\ 2}$) which are 103 V and 76 V, respectively, verifying (19) and (20). Similar to the step-up mode, the voltage spike can be suppressed. Fig. 9 (c), (d) and (e) show the voltage waveforms and current waveforms of the diodes $D_{\ 1}$, $D_{\ 2}$, and $D_{\ 3}$, respectively. (16), (17) and (18) are evidenced with the voltage stresses of $V_{D\ 1}, V_{D\ 2}$, and $V_{D\ 3}$ which are about 103 V, 103V, and 180 V. Considering the parasitic capacitor of diode $D_{\ 2}$, the voltage of $D_{\ 2}$ will resonate with the leakage inductor on the secondary side of the coupled inductor, also affecting the primary side current of the coupled inductor. Therefore, the current of L_k has resonance phenomena during the rising time. Moreover, the value of $i_{D\ 2}$ is related to the slope of currents of L_m and L_k . In both step-up and step-down modes, the currents of L_m and L_k have significant differences so that $i_{D\ 2}$ has different waveforms. The voltages and currents of the semiconductor have resonance phenomena because L_k resonates with the parasitic capacitance of the semiconductor at the turn-off time of power switches.

The experimental results in the closed-loop for output voltage under both step-up and step-down modes are given in Fig. 10 (a) and (b), respectively. The load current changes from 50% of the rated value to 100% and then back to 50% of the rated value. The stability performances of the dynamic response are presented.

Fig. 11 (a) and (b) show the block diagram of power losses distributions in step-up mode under $V_{in} = 15$ V, $V_o = 48$ V, and $P_o = 100$ W and step-down mode under $V_{in} = 75$ V, $V_o = 48$ V, and $P_o = 100$ W, respectively. Both of these modes, the diodes loss is the highest part of the total losses. To improve the efficiency, the lower forward voltage drops and resistance of diodes can be selected.

The curves of measured efficiency versus output power in both step-up and step-down modes are plotted in Fig. 12. The maximum efficiency when the converter operates in the step-up mode and step-down mode are 95.7% and 96.8%, respectively. The full load efficiency of the step-up mode and step-down mode are 86.8% and 96.2%, respectively.

Table the experimental parameters

Parameter	Type & Value
Input voltage (V_{in})	15 V˜75 V
Output voltage (V_o)	48 V
Rated output power (P_o)	100 W
Switching frequency (f_s)	100 kHz
Capacitors (C_1, C_2, C_o)	C_1 & C_2: 100 µF C_o: 220 µF
Power diodes (D_1, D_2, D_3)	D_1 & D_2: MBR20300 D_3: IDH10G65
Power switches (S_1, S_2)	IPP110N20N
Inductor (L_1)	155 µH Ferrite core PQ3230 Material PC95
Magnetizing inductor (L_m)	121 µH Ferrite core EE4220 Material PC40
Leakage inductor (L_k)	1.69 µH
Turns ratio ($N_p : N_s$)	20:20

(a) (b)

Fig. The voltage gain versus the duty cycle with various turns ratio under (a) step-up and step-down mode; (b) step-down mode.

(a) (b)

(c) (d)

(e)

Fig. Experiment waveforms under boost mode at $V_{in} = 15$V, $V_o = 48$V and $P_o = 100$W (a) $V_{gs\ 1}, V_{gs\ 2}, V_{ds\ 1}$, i_{L1} ; (b) $V_{gs\ 1}, V_{ds\ 2}$, i_{Lk} ; (c) $V_{gs\ 1}, V_{D\ 1}$, i_{D1} ; (d) $V_{gs\ 1}, V_{D\ 2}, i_{D\ 2}$; (e) $V_{gs\ 1}, V_{D\ 3}, i_{D\ 3}$.

(a) (b)

(c) (d)

(e)

Fig. Experiment waveforms under boost mode at $V_{in} = 75\text{V}, V_o = 48\text{V}$ and $P_o = 100\text{W}$ (a) $V_{gs\ 1}, V_{gs\ 2}, V_{ds\ 1}$, i_{L1} ; (b) $V_{gs\ 1}, V_{ds\ 2}$, i_{Lk} ; (c) $V_{gs\ 1}, V_{D\ 1}$, i_{D1} ; (d) $V_{gs\ 1}, _{VD\ 2}$, $i_{D\ 2}$; (e) $V_{gs\ 1}, V_{D\ 3}, i_{D\ 3}$.

(a) (b)

Fig. Closed-loop experimental results in (a) Boost mode; (b) Buck mode.

(a) (b)

Fig. 11 Block diagram of power losses distributions in (a) step-up mode (b) step-down mode.

Fig. The curves of measured efficiency versus output power in both step-up and step-down modes.

CONCLUISION

In this article, a coupled inductor buck-boost converter based dual switches is presented. The circuit has many advantages are as follow: (1) combing the passive clamp circuit to suppress the generation of power switching voltage spikes and recover the leakage energy; (2) the high voltage gain and wide conversion ratio can be achieved by changing the turns ratio of the coupled inductor and duty cycle; (3) common ground between input sources and load; (4) continuous input current. Steady-state analysis and design of components are presented in detail. Power loss analysis and comparison with some key characteristics of other converters are also presented and discussed. Finally, the results of the implemented prototype verify the correctness of the theoretical analysis, while the maximum efficiency in step-up mode and step-down mode are 95.7% and 96.8%, respectively.

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