A Wide Input Voltage Range, High PSR Low-Dropout Regulator with a Closed-Loop Charge Pump for Sensor Front-End Circuits

Zhiwen Niu[1], Xinquan Lai[1], and Bingyuan Wang[1]

[1]Xidian University Department of Electronic Engineering

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A Wide Input Voltage Range, High PSR Low-Dropout Regulator with a Closed-Loop Charge Pump for Sensor Front-End Circuits†

Zhiwen Niu*[1,2] | Xinquan Lai[1,2] | Bingyuan Wang[1,2]

[1]Institute of Electronic Computer-Aided Design, Xidian University, Shaanxi, China
[2]Key Laboratory of High-Speed Circuit Design and Electromagnetic Compatibility, Ministry of Education, Shaanxi, China

Correspondence
*Zhiwen Niu, Xidian University, No. 2 South Taibai Road, Xi'an, Shaanxi,China.
Email: niuzhiwen4213@126.com

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Summary

This paper presents a low dropout regulator (LDO) with a wide input voltage range and high power supply rejection (PSR) for Hall sensor front-end circuits, which is fabricated with a 0.18 μm BCD process. A topology in which a closed-loop charge pump biases the gate of two-stage cascode NMOS pass transistors is proposed to increase immunity to Electro-Magnetic Interference (EMI) capability for automotive applications. Furthermore, a power-down protection circuit is proposed to maintain the reliability of the system, and a novel implementation of the charge pump unit is presented to improve the influence of the body effect. Detailed derivation regarding the analyses of the simplified small-signal model of the closed-loop charge pump, the loop stability, and the PSR at various frequency bands is given. Simulation and measurement results show that the proposed LDO can operate with the input voltage from 5 V to 40 V, providing up to 60 mA current drive capability, and its minimum operating voltage is 2.5 V with a 10 mA load capacity. Moreover, results verify that measured PSR is better than -45 dB at 1.5 kHz, and measured PSR is better than -30 dB at 15 MHz. The results confirm that the obtained parameters of line and load regulations are significantly improved to 1.86 mV/V and 1.75 mV/mA, respectively.

KEYWORDS:
Low dropout regulator (LDO), Wide input voltage range, Closed-loop charge pump, Power-down protection, Power supply rejection (PSR)

1 | INTRODUCTION

Nowadays, with the rapid development of system-on-chip (SOC) technology, low dropout regulators (LDOs) have been widely used in industrial and automotive electronics[1,2,3], and it is possible to integrate the LDOs and their load circuits on the same die. It not only miniaturizes the size of the modules but also reduces non-ideal noise caused by the bonding wires and printed circuit boards (PCB) traces[4]. In particular, for noise-sensitive circuits such as Hall sensor analog front-end circuits, a well-regulated voltage is essential to ensure high immunity to power supply variations caused by switching ripple and noise in power management[5,6,7]. Moreover, sensing elements and their signal conditioning circuits in automotive applications are highly susceptible to crosstalk ripple interference due to the complex electromagnetic environment[8]. Therefore, it is vital to realize the high power supply rejection (PSR) of on-chip LDOs for accurate amplification of weak magnetic signals. Besides, in typical automotive applications, a wide input voltage range of 5 V to 30 V and an extensive operating temperature range of -40 ℃ to

†This is an example for title footnote.
[0]**Abbreviations:** ANA, anti-nuclear antibodies; APC, antigen-presenting cells; IRF, interferon regulatory factor

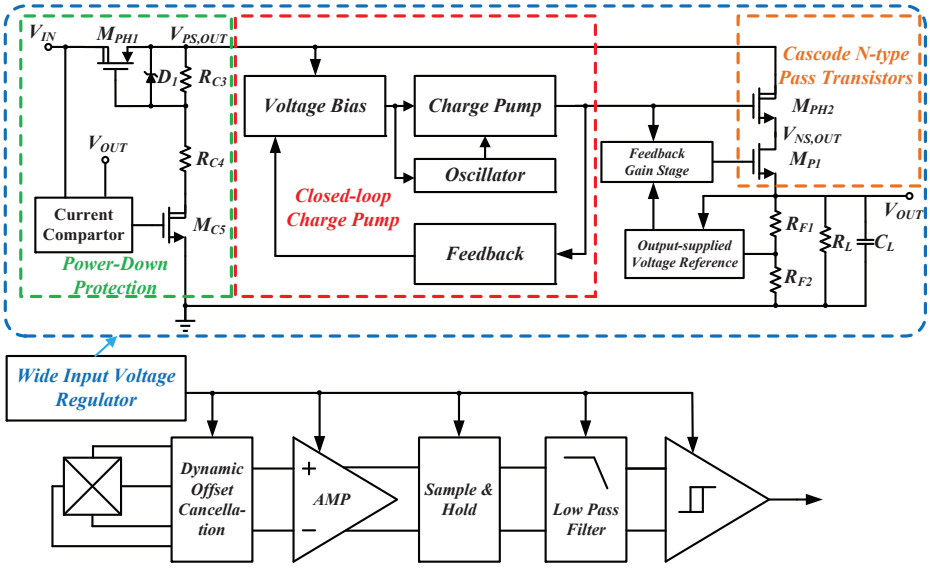


Figure 1 Schematic of the Hall sensor analog front-end circuits containing a proposed on-chip LDO

150 ℃ are required. However, for most LDOs with a typical input voltage range, the input and output voltage are close[9]. As a result, it is critical to meet both requirements of a wide operating voltage range and high PSR for automotive applications.

Prior research has made significant strides in enhancing the PSR of LDOs through various approaches. Generally, the PSR of LDOs is dependent on the bandwidth of the feedback paths, DC gain of the gain stages, and output transconductance of the pass transistors[10]. For instance, a feed-forward approach was proposed to broaden the PSR bandwidth by introducing the power-side ripple to the gate or body of the pass transistor, offsetting the additional ripple generated at the output[8,11,12,13]. However, this method requires a wide bandwidth of the feed-forward amplifier to acquire the power-side high-frequency ripple, consuming more bias currents. Another method involves pre-regulating the supply voltage to isolate the drain voltage of the pass transistor from the supply voltage[6], which introduces a negative feedback loop to respond to load current changes. However, the capacitive coupling of this method makes the start-up circuit sensitive to the process. Meanwhile, a technique with multiple feedback loops and gain stages has also been employed to achieve wide bandwidth and high DC gain[14,15,16,17], which improves the PSR and response speed. The introduction of multiple gain stages leads to increased power consumption and complexity of loop stability compensation. In addition, the cascode of the pass transistors was proposed to enhance PSR by increasing the output impedance, such as two-stage cascode transistors[18] and three-stage cascode transistors[19]. Among them, an open-loop charge pump is employed to provide bias voltage for the gate of the N-type pass transistors, which can reach better noise isolation. However, the minimum operating voltage of the circuit is limited due to the drop voltage of multiple pass transistors and the open-loop charge pump is more sensitive to the change of power supply. Furthermore, a circuit architecture was proposed that includes a reference circuit provided by the output voltage of the regulator, which ensures that the voltage difference across the input of the error amplifier is free from any tiny ripple introduced by the supply voltage[20]. It is worth noting that the LDO startup process requires careful consideration to prevent improper circuit setup.

Moreover, previous research has also focused on expanding the input voltage range of LDOs. One proposed method used a slew-rate booster and frequency compensation circuit composed of bipolar devices to reduce the circuit sensitivity to the supply variations from 5.25 V to 40 V[9]. However, the use of bipolar devices results in a larger die area. For high-voltage supply SOC applications, a dynamic compensation network is presented to achieve stable performance for the voltage range from 4 V to 40 V[21]. Similarly, a pre-regulator method with a negative feedback loop was designed to achieve high PSR, and the circuit can operate within an input voltage range of 5.5 V to 40 V[22]. Meanwhile, a self-referenced architecture was proposed with a current mirror-based power stage to expand the input voltage range to 12 V, and achieve a PSR of -40 dB at 50 kHz[23]. All three methods require an off-chip capacitor no smaller than 1 uF, which reduces the bandwidth of the LDO and increases the response time. Besides, a feedforward compensated design that isolates the input voltage from the power supply of the amplifier was proposed, which can operate from 69 V to 75 V[24]. Unfortunately, the feedback resistors in this design require a current consumption of almost 120 μA, which is almost half of the total quiescent current.

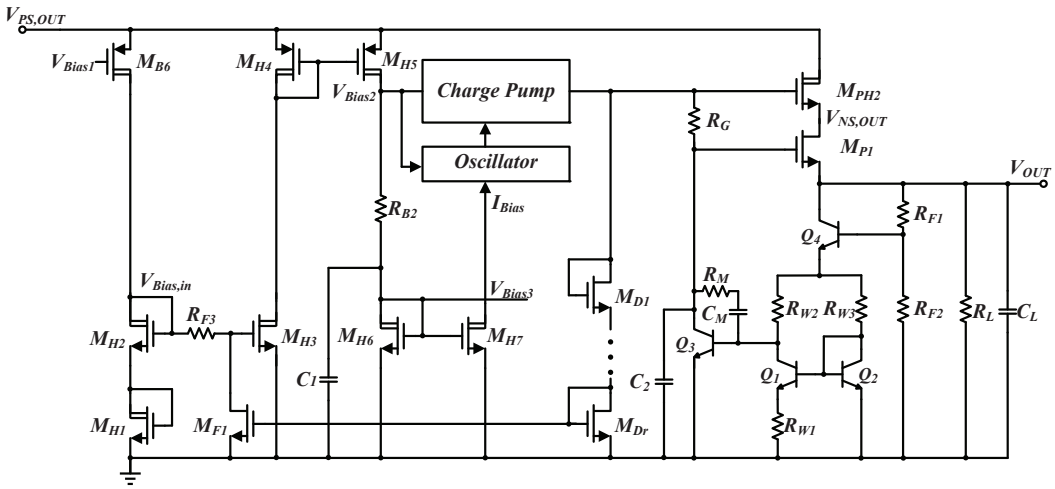


Figure 2 The architecture of the proposed LDO

Different from the above work, we target automotive applications requiring a wide operating voltage range and high PSR on-chip LDO. It means that the pass transistors need enough gate-source voltage at low input voltage and the circuits will not crash at high input voltage. For conventional LDOs with N-type pass transistors, a level shift circuit is used to bias the gate voltage or a charge pump circuit is employed to supply the amplifier[19]. However, the charge pump is more sensitive to the change in power supply due to the limitation of open-loop architecture. In addition, the area of the amplifier is greatly increased due to the use of high-voltage transistors, especially in the cascaded transistor structure, where the area is doubled.

Therefore, this paper presents a topology that employs a closed-loop charge pump to bias the gate voltage of two-stage cascode N-type pass transistors. And an improved Wildar's voltage reference circuit supplied by the output voltage of LDO replaces the conventional amplifier to reduce the area and power dissipation. Furthermore, a power-down protection circuit is proposed to enhance system reliability.

The rest of this paper is organized as follows. Section II discusses the architecture of the proposed LDO and presents a detailed analysis of the closed-loop charge pump, including small-signal, stability, and PSR analysis. In Section III, the design of various circuits of the proposed LDO, such as the power-down protection circuit, bias circuit, oscillator circuit, closed-loop charge pump circuit, and improved voltage reference circuit are described. Section IV presents the experimental results that verify the function and performance of the fabricated LDO and provides a performance comparison with other works. Finally, Section V concludes the paper.

2 | PROPOSED LDO ARCHITECTURE

In this section, the architecture and analysis of the proposed LDO to improve PSR are presented.

2.1 | Proposed LDO Architecture

Figure 1 shows the block diagram of a hall front-end circuit that incorporates the proposed on-chip LDO. It comprises several key components, including a power-down protection circuit, a closed-loop charge pump, two cascode NMOS pass transistors, an output-supplied voltage reference, and a feedback loop, as previously described. Specifically, a current comparator is utilized to detect a brownout state, which immediately shuts down M_{PH1} to prevent current backflow from the output node to the input node. To address low input voltage conditions, a topology is proposed where a regulated charge pump biases two-stage cascode pass transistors. Figure 2 illustrates a visual representation of the proposed LDO for a wide input voltage range. Generally speaking, the pass transistors of LDO work in the saturation region. However, in order to provide a large load current, the size of the pass transistors is larger. Therefore, there may be the possibility of the pass transistors working area changing under the condition of different loads. Especially under light load conditions, the transistor may operate in the subthreshold region. In this paper, the charge pump supplies sufficient bias voltage to the gate voltage of the high voltage and standard voltage NMOS pass

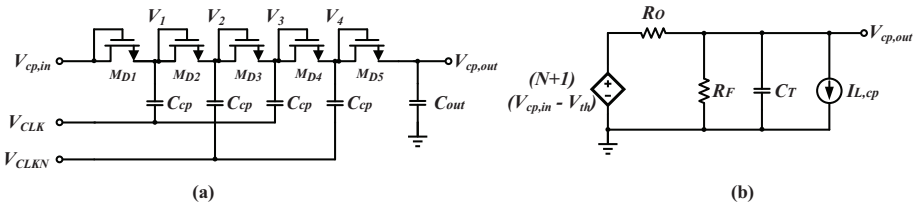


Figure 3 (a) Architecture and (b) Simplified model of the traditional open-loop four-stage Dickson charge pump

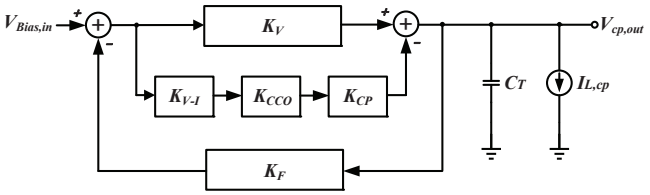


Figure 4 Simplified model of the proposed closed-loop charge pump.

transistors, allowing them to withstand high voltages and accommodate a broad input range from 2.5 V to 40 V. Besides, $V_{bias,in}$ is generated by two diode-connected NMOS transistors, M_{H1} and M_{H2}, and the voltage value is determined by the bias current which is insensitive to the power supply. The second-stage NMOS pass transistor, Wildar's voltage reference, and feedback loop work together to form an op-amp-less regulator, where the voltage reference circuit's power supply is provided by the output. Since the Hall sensor circuit with a power consumption of 3 mA, the minimum load current of the proposed on-chip LDO is 3 mA. Both M_{PH2} and M_{P1} remain in the saturation region, effectively blocking power supply noise and ripple, regardless of the load current's magnitude.

Besides, a closed-loop charge pump is designed to regulate the input voltage and pump frequency based on the output voltage, effectively maintaining a constant gate-source voltage of M_{PH2} and isolating the input and output voltages. The output voltage of the charge pump is sensed by a series connection of diode-connected transistors, $M_{D1} - M_{Dr}$ (r=11), while its input voltage is dynamically adjusted by the negative feedback resistor R_{F3}. By incorporating Wildar's voltage reference circuit, the proposed regulator circuit is significantly enhanced. The value of the output voltage is 2.45V, and the output voltage of the regulator is given by

$$V_{OUT} = \frac{R_{F1} + R_{F2}}{R_{F2}} \cdot (2V_{BE} + \frac{R_{W3}}{R_{W1}} \cdot V_T \ln n). \tag{1}$$

2.2 | Analysis of the Proposed Closed-loop Charge Pump

Figure 3(a) shows the application of a traditional four-stage Dickson charge pump in an open-loop architecture[25], the output voltage of this charge pump is

$$V_{cp,out} = V_{cp,in} - V_{th} + N \cdot (V_{CLK} - V_{th} - \frac{I_{cp,out}}{C_{cp} \cdot f_{CLK}}), \tag{2}$$

where V_{th} is the MOS threshold voltage, N is the value of stage, f_{CLK} is the pumping frequency, and $I_{cp,out}$ is the load current.

It should be noted that Equation (2) shows the output voltage of the charge pump is influenced by multiple factors, and any change in these factors will ultimately the gate bias voltage of the M_{PH2} and M_{P1}. In this paper, since the power supply of the oscillator and the input of the charge pump are the same nodes, $V_{cp,in}$ and V_{CLK} are equal. Figure 3(b) shows a simplified model of an open-loop charge pump, which is equivalent to an RC circuit[25].

To facilitate the analysis, an equivalent model is used to describe the charge pump in a closed-loop state, because the nonlinear changes in output impedance and feedback coefficients make the analysis more complex compared to that of the charge pump in an open-loop state. As shown in Figure 4, a simplified model of the proposed closed-loop charge pump is adopted. Among them, the loop gain, K, consists of constant gains, K_V and K_F, defined by the stage of charge pump and the feedback resistor R_{F3}, a conversion gain, K_{V-I}, from input voltage to bias current, a conversion gain, K_{cco}, of the current-controlled oscillator

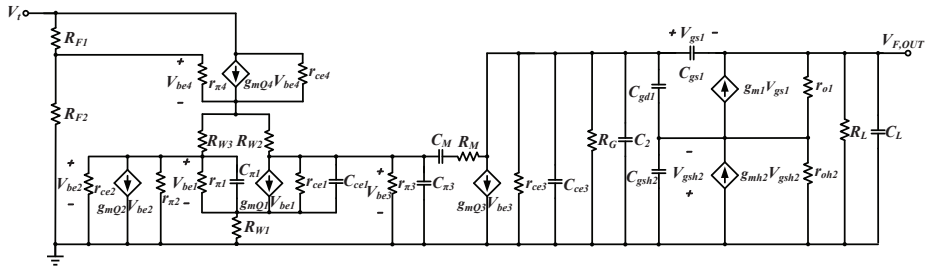


Figure 5 Simplified small-signal equivalent circuit diagram of the proposed LDO in open-loop state

(CCO) from current to frequency, and a conversion gain K_{cp}, of the charge pump from frequency to voltage.

$$K = K_F \cdot (K_V - K_{V-I} \cdot K_{cco} \cdot K_{cp}) \tag{3}$$

$$K_F = gm_{F1} \cdot (R_{F3} + 1/gm_{H1} + 1/gm_{H2})/r. \tag{4}$$

$$K_{cco} = 2\pi\partial f_{CLK}/\partial I_{cco} = \pi/(C_{O1} \cdot (V_{CLK} - V_M)). \tag{5}$$

$$K_{cp} = \partial V_{cp,out}/\partial f_{CLK} = \frac{N \cdot I_{cp,out}}{C_{cp} \cdot f_{CLK}^2}. \tag{6}$$

where,I_{cco} is the bias current of the oscillator, C_{O1} is the capacitor of the oscillator in Figure 8(a), V_M is flip voltage of the inverter, and r means the number of voltage divider resistors. So

$$K \approx \frac{gm_{F1}R_{F3}}{r} \cdot (N + 1 - K_{V-I} \cdot \frac{N \cdot \pi}{C_{O1} \cdot (V_{CLK} - V_M)} \frac{I_{cp,out}}{C_{cp} \cdot f_{CLK}^2}). \tag{7}$$

As can be seen from the above equation, there are many variables that determine the value of the loop gain. As the unwanted load current increases, the loop gain decreases. Therefore, there is a trade-off between the loop gain of the charge pump and the bandwidth of the regulator's loop. It is worth noting that there will be a small ripple voltage V_R at the output of the charge pump in open-loop architecture, which is defined as

$$V_R = I_{cp,out}/f_{CLK}C_{out}. \tag{8}$$

The values of C_{out} and f_{CLK} should be larger, and the load current, $I_{cp,out}$, should be smaller. However, when the charge pump works in closed-loop architecture, the f_{osc} is adjusted by the variation of load current. According to Equation (2),

$$f_{osc} = \frac{N \cdot I_{cp,out}}{C_{cp} \cdot ((N + 1)(V_{cp,in} - V_{th}) - V_{cp,out})}. \tag{9}$$

Thus, the ripple voltage, V_R, at the output in closed-loop architecture is

$$V_R = \frac{C_{cp}((N + 1)(V_{cp,in} - V_{th}) - V_{cp,out})}{N \cdot C_{out}}. \tag{10}$$

Notably, the ripple in the proposed closed-loop architecture is independent of $I_{cp,out}$ and f_{osc}. The value of C_{out} should be larger, thereby reducing the ripple at the output and increasing PSR. However, larger output capacitors mean a slower time to reach a steady state.

2.3 | Analysis of the Stability

To analyze the stability performance of the low dropout regulator, the feedback loop can be opened at the output node to calculate the loop gain and obtain the open-loop transfer function. Assuming constant power supply voltage and load current, the output voltage of the charge pump remains relatively stable in the steady state, and can be approximated as the bias voltage for the gate of M_{PH2}. Additionally, the pole caused by the parasitic capacitance of M_{PH2} does not affect the feedback loop. To simplify the calculation, Figure 5 depicts an open-loop small-signal equivalent circuit diagram. Due to the closed-loop characteristic of the charge pump, closed-loop impedance R_{CL} is suppressed by the loop gain. Therefore, the output of the charge pump can be

simplified to a small grounded AC signal. In addtion, the load equivalent impedance seen at V_t is high, so the effect of this load is negligible at the output node seen at $V_{F,OUT}$. The resulting open-loop transfer function is given below:

$$\begin{aligned}\frac{V_{f,out}}{V_t}(s) &= A_0 \cdot \frac{1 - sC_M/g_{mQ3}}{1 + s((C_{\pi 3} + C_{ce1} + C_M(1 + A_1))(r_{\pi 3}//R_{W2}))} \cdot \frac{1 + sC_{gsh2}/g_{mh2}}{1 + sC_2(R_G//r_{ce3})} \cdot \frac{1 + sC_{gs1}/g_{m1}}{1 + sC_L(R_L//(\frac{1}{g_{m1}} + \frac{1}{g_{mh2}}))} \cdot \\ &= A_0 \cdot \frac{(1 + s/w_{z1})(1 + s/w_{z2})(1 + s/w_{z3})}{(1 + s/w_{p1})(1 + s/w_{p2})(1 + s/w_{p3})},\end{aligned} \tag{11}$$

where,

$$A_0 = \frac{r_{\pi 3}}{R_{W2} + r_{\pi 3}} \cdot \frac{R_{F2}}{R_{F1} + R_{F2}} \cdot g_{mQ3} \cdot (R_G//r_{ce3}) \tag{12}$$

$$k = \frac{r_{\pi 3}}{R_{W2} + r_{\pi 3}} \cdot \frac{R_{F2}}{R_{F1} + R_{F2}} \tag{13}$$

$$A_1 = g_{mQ3} \cdot (R_G//r_{ce3}) \tag{14}$$

$$w_{p1} = \frac{1}{(C_{\pi 3} + C_{ce1} + C_M(1 + A_1))(r_{\pi 3}//R_{W2})} \approx \frac{1}{C_M(1 + A_1)(r_{\pi 3}//R_{W2})}, \tag{15}$$

$$w_{p2} = \frac{1}{C_2(R_G//r_{ce3})}, \tag{16}$$

$$w_{p3} = \frac{1}{C_L(R_L//(\frac{1}{g_{m1}} + \frac{1}{g_{mh2}}))} \approx \frac{g_{m1}g_{mh2}}{C_L(g_{m1} + g_{mh2})}, \tag{17}$$

$$w_{z1} = g_{mQ3}/C_M, \tag{18}$$

$$w_{z2} = -g_{m1}/C_{gs1}, \tag{19}$$

$$w_{z3} = -g_{mh2}/C_{gsh2}, \tag{20}$$

Despite the negative feedback loop being introduced, the switching noise and ripple from the charge pump can still affect the gate of the M_{PH2} and M_{P1}. Additionally, the noise present in the power supply may also couple to the gate of the M_{PH2} via the parasitic gate-drain capacitance, C_{gd}. Therefore, to suppress the switching noise of the charge pump, a first-order low-pass filter (LPF) is inserted between the output of the charge pump and the gate of the M_{P1}, consisting of R_G and C_2. As shown in Equation (12), R_G should be as large as possible to provide a large loop gain.

Equation (11) reveals the existence of three poles and three zeros in the system, with W_{p1} as the dominant pole and W_{z1} as the right half-plane zero due to the Miller capacitor C_1. A resistor R_M is introduced to adjust the position of the right half-plane zero to the location of the second pole in the left half-plane, thus canceling out their respective impacts on the gain and phase shift. However, the presence of R_M introduces an additional pole whose position is usually high frequency and is therefore ignored. It is noteworthy that the presence of cascode pass transistors shifts W_{p3} to a lower frequency. This is due to the cascode of the M_{PH2} and M_{P1}, which increases the equivalent output impedance. To ensure system stability, the non-dominant pole must maintain a phase margin greater than 60°. Additionally, the gain bandwidth (GBW) is expressed as

$$GBW = g_{mQ3}/(C_M + C_2). \tag{21}$$

2.4 | Analysis of the PSR

As mentioned above, the gate voltage of the NMOS pass transistors is biased by the output of the charge pump, and the power supply ripple is primarily coupled to $V_{NS,OUT}$ via two paths. The first path involves coupling $V_{PS,OUT}$ to $V_{NS,OUT}$ through the r_{oh2} of the M_{PH2}, while the second path involves the coupling of parasitic capacitances, such as C_{gdh2} and C_{gsh2} of M_{PH2}. Similarly, the power supply ripple is mainly coupled to V_{OUT} from $V_{NS,OUT}$ through two paths. The first path involves the coupling of $V_{NS,OUT}$ to V_{OUT} through r_{o1} of the M_{P1}, while the second path involves the coupling of C_{gd1} and C_{gs1}. To facilitate the analysis of PSR, a simplified small-signal model is presented in Figure 6.

$$PSR = \frac{V_{out}}{V_{in}}(s) = \frac{V_{out}}{V_{ps,out}}(s) = \frac{V_{out}}{V_{ns,out}}(s) \cdot \frac{V_{ns,out}}{V_{ps,out}}(s), \tag{22}$$

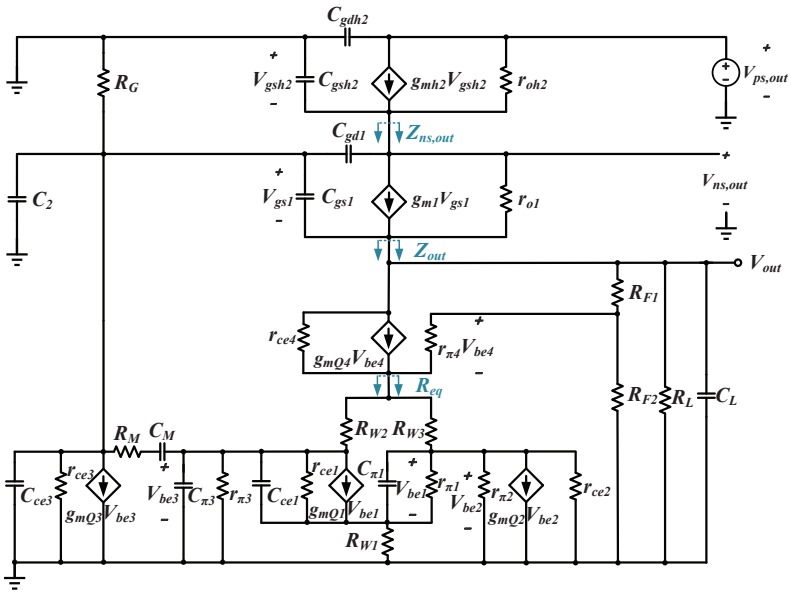


Figure 6 Simplified small-signal model for analyzing PSR.

where, $V_{ps,out}$, $V_{ns,out}$ and V_{out} are small signals respectively, and the PSR of the regulator can be calculated in steps by $V_{out}/V_{ns,out}$ and $V_{ns,out}/V_{ps,out}$. For the convenience of calculation, the equivalent output impedance of V_{out} and $V_{ns,out}$ can be obtained. Z_{out} is the equivalent output load, which is

$$Z_{out} = \frac{R_{W3}//(R_{W2}+r_{\pi3})}{R_{F2}+R_{W3}//(R_{W2}+r_{\pi3})}(R_{F2}+R_{F1})//R_L//\frac{1}{sC_L}. \tag{23}$$

The $V_{out}/V_{ns,out}$ is given

$$\frac{V_{out}}{V_{ns,out}} = \frac{sC_{gd1}+\frac{sC_{eq1}+\frac{1}{R_G//r_{ce3}}}{(g_{m1}+sC_{gs1})r_{o1}}}{\frac{1}{R_G//r_{ce3}}+kg_{mQ3}+s(C_{eq1}-C_{gs1})+\frac{sC_{eq1}+\frac{1}{R_G//r_{ce3}}}{(g_{m1}+sC_{gs1})(Z_{out}//r_{o1})}}, \tag{24}$$

where, $C_{eq1} = C_{gs1}+C_{gd1}+C_{ce3}+C_2$. And the $V_{ns,out}/V_{ps,out}$ is given

$$\frac{V_{ns,out}}{V_{ps,out}} = \frac{1}{(g_{mh2}+\frac{1}{Z_{ns,out}}+sC_{gsh2})r_{oh2}+1}, \tag{25}$$

where, since the same current flows through the $V_{NS,OUT}$ node and the V_{OUT} node, there can be

$$Z_{ns,out} = \frac{V_{ns,out}}{V_{out}}\cdot Z_{out}. \tag{26}$$

According to the above equation, PSR is obtained

$$PSR = \frac{sC_{gd1}+\frac{sC_{eq1}+\frac{1}{R_G//r_{ce3}}}{(g_{m1}+sC_{gs1})r_{o1}}}{\frac{1}{R_G//r_{ce3}}+kg_{mQ3}+s(C_{eq1}-C_{gs1})+\frac{sC_{eq1}+\frac{1}{R_G//r_{ce3}}}{(g_{m1}+sC_{gs1})(Z_{out}//r_{o1})}}\cdot\frac{1}{(g_{mh2}+\frac{1}{Z_{ns,out}}+sC_{gsh2})r_{oh2}+1}. \tag{27}$$

At different frequencies, the main factors that affect the performance of PSR are variable. As the frequency approaches zero,

$$PSR|_{f=0} \approx \frac{1}{kg_{mQ3}(R_G//r_{ce3})g_{m1}r_{o1}g_{mh2}r_{oh2}}. \tag{28}$$

As can be seen from equation (28), compared with a single pass transistor, the cascoding transistors improves the PSR at DC frequency. Consequently, at low frequencies, $g_{m1}r_{o1}$ and $g_{mh2}r_{oh2}$ should be as large as possible. At this time, the loop gain of the regulating loop is large enough. As the frequency increases, the loop gain decreases, and when the frequency is less than

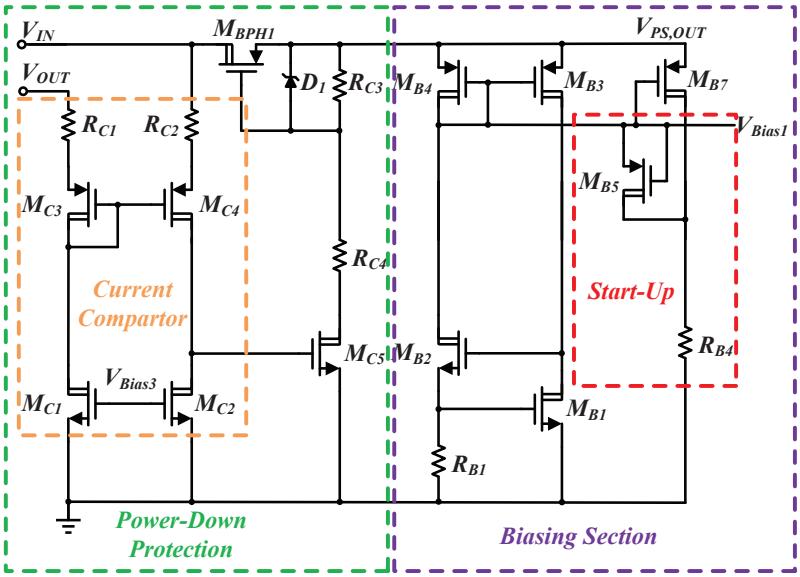


Figure 7 The conceptual architecture of the power-down protection circuit, start-up and biasing circuit

GBW, PSR can be expressed as

$$PSR|_{f<GBW} = \frac{sC_{gd1} + \frac{sC_{eq1}+\frac{1}{R_G//r_{ce3}}}{g_{m1}r_{o1}}}{\frac{1}{R_G//r_{ce3}} + kg_{mQ3} + s(C_{eq1} - C_{gs1}) + \frac{sC_{eq1}+\frac{1}{R_G//r_{ce3}}}{g_{m1}(Z_{out}//r_{o1})}} \cdot \frac{1}{(g_{mh2} + sC_{gsh2})r_{oh2}}. \tag{29}$$

At this time, Z_{out} is defined as

$$Z_{out} = \frac{R_{W3}//(R_{W2} + r_{\pi 3})}{R_{F2} + R_{W3}//(R_{W2} + r_{\pi 3})}(R_{F2} + R_{F1})//R_L. \tag{30}$$

Equation (29) shows that PSR is related to many parameters, in which the larger g_{mQ3}, g_{mh2}, r_{oh2} and C_2 are, the better the PSR is. Moreover, the value of C_{gd1} should be as small as possible and C_{gsh2} should be as large as possible, which means that the size of M_{PH2} should be larger than that of M_{P1}.

When the frequency is greater than GBW, Z_{out} is 1/ (sC_L), so $Z_{ns,out}$ is approximately equal as

$$Z_{ns,out} \approx \frac{C_{eq1}/(C_L//C_{gs1}) - C_{gs1}/C_L}{sC_{gd1}}. \tag{31}$$

PSR can be expressed as

$$PSR|_{f>GBW} = \frac{1}{s(\frac{C_{eq1}-C_{gs1}}{C_{gd1}} + \frac{C_{eq1}C_L}{C_{gd1}C_{gs1}})(\frac{C_{gsh2}}{C_{gd1}} + \frac{C_{gs1}}{C_{eq1}})r_{oh2}} \tag{32}$$

Equation (32) indicats that when the frequency is high, the value of PSR is strongly related to the parasitic capacitance and the load capacitance. Among them, increasing the load capacitance C_L and C_2 will effectively improve the PSR. However, this means slower response times. And larger C_{gsh2} and smaller C_{gd1} can also improve PSR at high frequencies.

3 | CIRCUIT IMPLEMENTATION

In this section, the circuit implementation of the proposed LDO is presented.

3.1 | Power-down Protection Circuit

To prevent the risk of power failure in a complex electromagnetic environment of automotive applications and ensure the normal operation of the low dropout regulator, a power down protection method is proposed. This method utilizes a current comparator

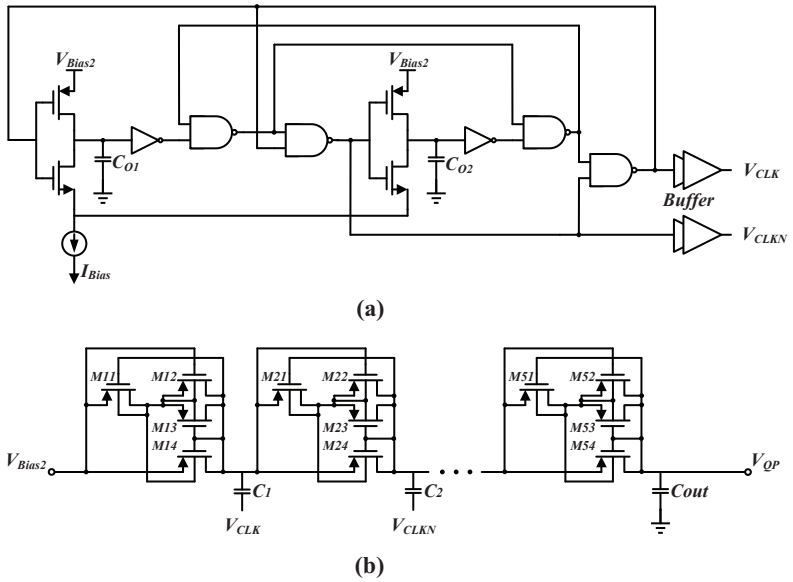


Figure 8 (a)Circuit of the applied current-control oscillator (b)The conceptual architecture of the proposed charge pump units

to continuously monitor the voltage of both input and output, where the value of R_{C1} and R_{C2} is equal. And the input voltage is typically greater than the output voltage when the regulator is functioning correctly. As a result, the gate-source voltage of M_{C4} is higher than that of M_{C3} and the current of M_{C4} is limited to the current of M_{C2}, while the gate voltage of M_{C5} is a high-resistance node, which enable M_{C5} to turn on. The resistor divider between R_{C3} and R_{C4} determines the gate source voltage of M_{PH1}, which is safeguarded by clamping diode D_1. When the input voltage drops momentarily below the output voltage, the gate-source voltage of M_{C4} drops rapidly. However, due to the presence of the output load capacitance C_L, the presence of the gate source voltageof M_{C3} still makes M_{C3} conductive. Since the gate voltage of M_{C5} is a high resistance node, it immediately drops and turns off M_{PH1}, preventing any backflow of current from the output node to the input node. It is worth noting that the arrow of M_{PH1} is towards the output, because the potential of $V_{PS,OUT}$ may be higher than that of V_{IN}, and a similar situation is also reflected in Figure 1.

3.2 | Start-up and Biasing Circuit

Figure 7 illustrates the start-up and self-biasing circuits, where M_{B1}, M_{B2} and R_{B1} work together to generate a bias current that is insensitive to the changes of the supply voltage[26]. Upon power-up, M_{B7} is conductive and current flows through R_{B4}, resulting in the drain voltage of M_{B5} increases and is higher than the source and gate voltage. Due to its diode connection, the current will vary from the drain flows to the source of M_{B5}, which separates the circuit from the merging point. Then the source and gate voltage is always higher than the drain voltage of M_{B5}, which means that the starting circuit has been completely closed. When $V_{PS} > 2V_{th} + V_{dsat}$, M_{B1}, M_{B2}, M_{B3}, and M_{B4} turn on. Resistor R_{B1}, which has a negative temperature coefficient, is used to produce a bias current with nearly zero temperature coefficient. The feedback loop formed by M_{B1} and M_{B2} helps to stabilize the value of the bias current. Moreover, since M_{B1} - M_{B7} are high-voltage transistors, their drain terminals can withstand high voltage input.

3.3 | Oscillator and Charge Pump

Figure 8(a) displays the circuit diagram of the applied CCO that generates the clock frequency for the charge pump. As previously mentioned, the clock frequency dynamically adjusts to the charge pump's output voltage by altering the bias current's magnitude. The current control gain, K_{cco}, is shown in formula (5). It is proportional to the oscillator output frequency and inversely proportional to the bias current. Compared with the traditional comparator based CCO, this oscillator uses inverter threshold voltage to control the current switch, and the delay time is greatly reduced. Besides, the structure can stably adjust the frequency of the charge pump to no more than its maximum frequency and make the charge pump vulnerable to limitation.

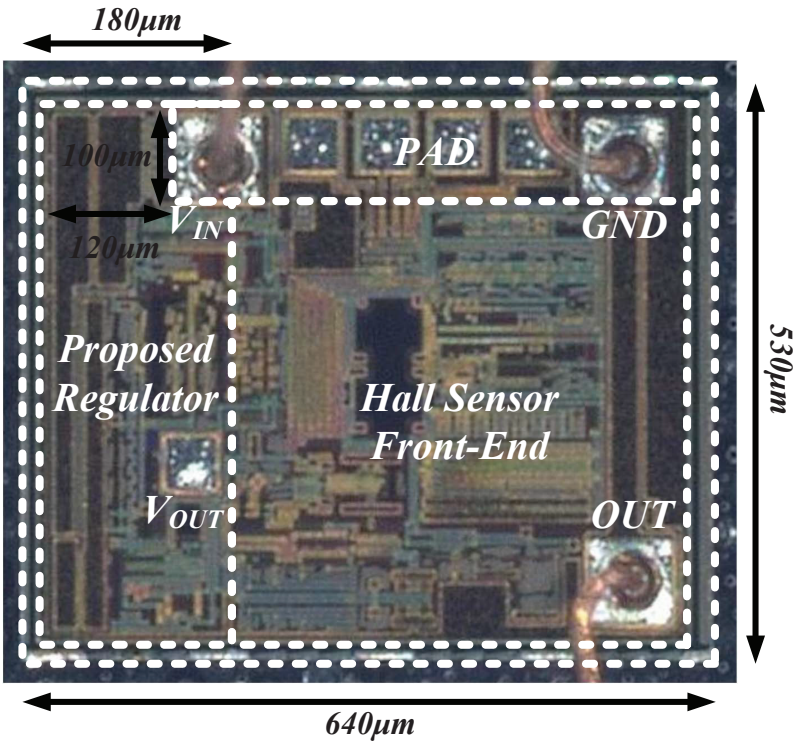


Figure 9 The chip microphotograph of the proposed LDO regulator with the hall sensor front-end circuit

Additionally, Figure 8(b) exhibits the proposed four-stage charge pump's schematic. Traditional Dickson charge pump generally uses NMOS transistor as the pumping unit, as shown in Figure 3 (a). However, the bulk of the NMOS transistor is connected to a P-sub in the standard CMOS process. On the one hand, this will lead to the breakdown of bulk-drain junction when the output voltage of charge is high. On the other hand, the body-effect of the lining NMOS transistor in the latter stage is larger, so the threshold voltage, V_{th} will change and ultimately affect the output voltage of charge pump.

Therefore, the PMOS transistor is used as the pump unit, and the bulk is connected with the source of PMOS transistor to eliminate the body-effect. More importantly, in the structure shown in Figure 8(b), the bulk of the M_{X1} - M_{X4} share a common potential, which is connected in a "suspended" n-well. Also, the voltage of the n-well is not less than the voltage of V_{in} and V_{out}, which prevents electrical leakage.

3.4 | Regulated Charge Pump and Improved Wildar's Voltage Reference Circuit

As shown in Figure 2, we propose a regulated charge pump circuit that employs a cascoded diode-connected transistor feedback network. By changing the gate-source voltage of M_{F1}, the negative feedback current can be altered, allowing control of the gate voltage of M_{H3}. This method is more efficient than using a structure with resistor network combined comparators since it saves area and has superior regulation capabilities. Additionally, M_{H7} supplies a bias current to the oscillator, while the charge pump's output generates sufficient bias voltage for the gate of M_{PH2} and M_{P1}. To implement the Wildar's voltage reference circuit, a feedback loop created by Q_3 and R_G is introduced, where this branch's current acts as the charge pump's load.

4 | SIMULATION AND MEASUREMENT RESULTS

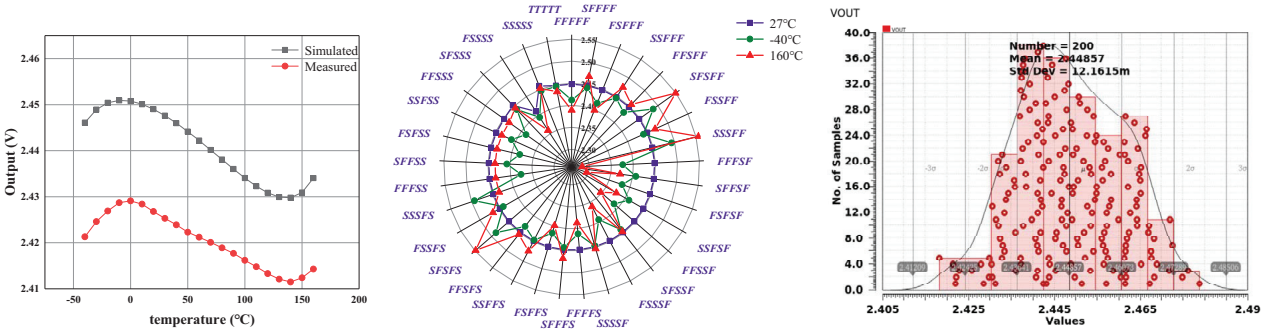
The proposed LDO regulator was manufactured using 0.18μm BCD technology, and its chip microphotograph is shown in Figure 9, revealing that the regulator's area is roughly 0.09 mm^2. The total current consumption, which includes the charge pump, results in a quiescent current, I_Q, of approximately 100 μA. Table 1 summarizes the width to length ratio of the transistors and Table 2 shows the values of resistors and capacitors in Figures 2 and 7.

Table 1 Transistor sizes of proposed LDO

Transistor	Size	Transistor	Size	Transistor	Size	Transistor	Size
MB1	12 µm/3 µm	MB2	12 µm/3 µm	MB3	16 µm/2 µm	MB4	16 µm/2 µm
MB5	4 µm/2 µm	MB6	8 µm/2 µm	MB7	4 µm/2 µm	MC1	3 µm/3 µm
MC2	3 µm/3 µm	MC3	8 µm/2 µm	MC4	8 µm/2 µm	MC5	12 µm/3 µm
MH1	6 µm/3 µm	MH2	6 µm/3 µm	MH3	6 µm/3 µm	MH4	8 µm/2 µm
MH5	16 µm/2 µm	MH6	6 µm/3 µm	MH7	24 µm/3 µm	MD1	5 µm/1 µm
MD2	5 µm/1 µm	MD3	5 µm/1 µm	MD4	5 µm/1 µm	MD5	5 µm/1 µm
MD6	5 µm/1 µm	MD7	5 µm/1 µm	MD8	5 µm/1 µm	MD9	5 µm/1 µm
MD10	5 µm/1 µm	MD11	5 µm/1 µm	MF1	5 µm/1 µm	MBPH1	2040 µm/2 µm
MPH2	3500 µm/3 µm	MP1	3500 µm/0.5 µm				

Table 2 Capacitors and Resistors values of proposed LDO

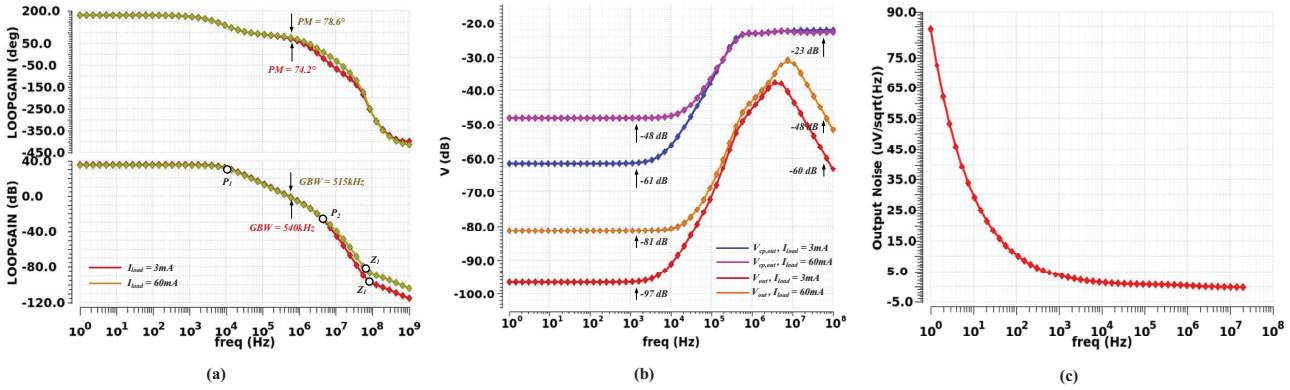
Device	Value	Type	Device	Value	Type
RB1	113 KΩ	Poly resistor	RB2	400 KΩ	Poly resistor
RC1	340 KΩ	Poly resistor	RC2	340 KΩ	Poly resistor
RC3	220 KΩ	Poly resistor	RC4	370 KΩ	Poly resistor
RG	2124 KΩ	Poly resistor	RW1	3.6 KΩ	Poly resistor
RW2	210 KΩ	Poly resistor	RW3	210 KΩ	Poly resistor
RF1	88 KΩ	Poly resistor	RF2	143 KΩ	Poly resistor
RF3	85 KΩ	Poly resistor	RM	5 KΩ	Poly resistor
C1	4000 fF	MOS capacitor	C2	200 fF	MOS capacitor
CM	270 fF	MOS capacitor			



(a) (b) (c)

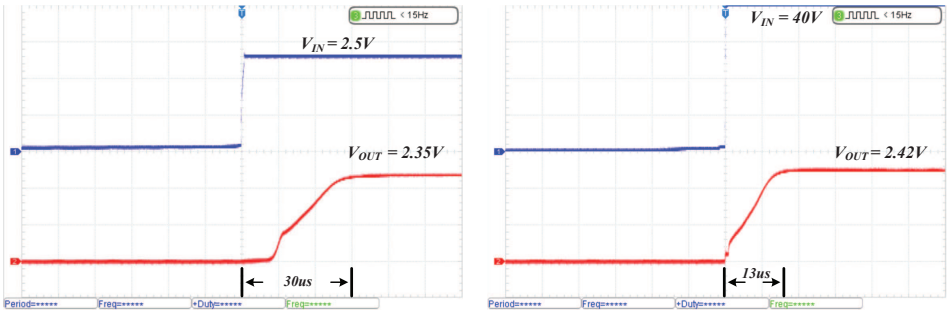
Figure 10 Simulation performance of output voltage with (a)temperature (b)corner and (c)Monte carlo

Figure 10 presents the robustness of the proposed LDO. Figure 10(a) shows the variation of LDO output voltage at the full temperature range through simulation and measurements. It can be seen that the difference between the maximum and minimum output of the proposed LDO in the full temperature range is less than 20 mV. Figure 10(b) exhibits the simulation results of the process corner. (Among them, TTTTT stands for nmos: typical, pmos: typical, Bipolar: typical, resistor: typical, and capacitor: typical.) It can be seen that the fluctuation of output voltage with high and low temperature is larger in different process corners. To evaluate the performance of the proposed LDO in the case of device and process mismatches, the Monte Caro simulation results are presented, and the statistical distribution of output voltage at room temperature is shown in Figure 10(c). The results present that when the mean output voltage is 2448.6 mV, the standard deviation is 12.16 mV.



(a) (b) (c)

Figure 11 Simulation performance of (a)frequency response (b)PSR and (c)Noise



(a) (b)

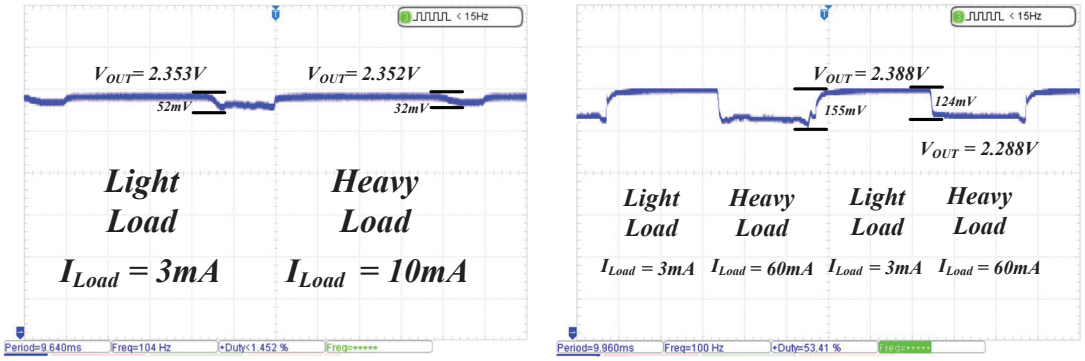
Figure 12 The measured transient response of the proposed regulator with (a)2.5 V start-up setting and (b)40 V start-up setting

Figure 11(a) presents the simulation results in the form of Bode plots, which demonstrate the loop's performance at load conditions of I_{load}=3 mA and 60 mA. The DC gain of the loop exceeds 35 dB, and the GBW is measured to be 540 kHz and 515 kHz, respectively, with a phase margin of 74.2° and 78.6°, which satisfies the necessary stability requirement for the feedback loop.

The simulation results of the proposed LDO regulator are further presented in Figure 11(b), showing the PSR curves at I_{load} = 3 mA and 60 mA, V_{IN} = 12V. It is observed that the PSR of the output is −97 and −81 dB at 1.5 kHz and attenuates as the frequency increases. However, in the high frequency, PSR is improved and reaches −60 and −48 dB at 15 MHz. Besides, the PSR of the charge pump is −61 and −48 dB at 1.5 kHz, and the PSR is around −23 dB at 15 MHz. Figure 11(c) shows the output noise characteristics of the proposed LDO regulator, and the RMS noise is 0.24μVrms.

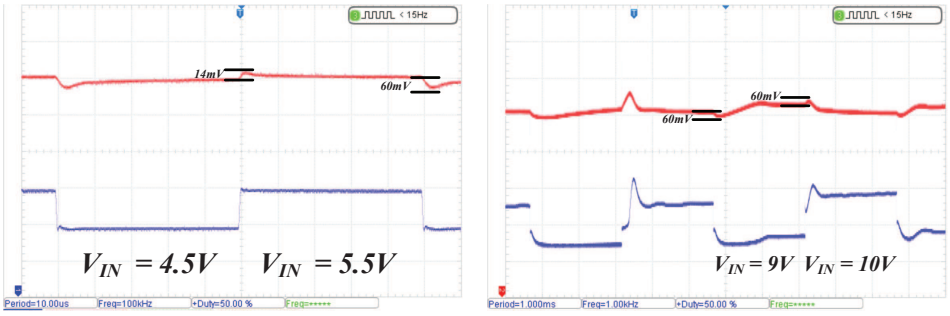
Additionally, the actual performance of the proposed LDO is validated through measurement results, as depicted in Figure 12, showcasing the transient response with (a) 2.5 V start-up setting and (b) 40 V start-up setting. These results show that when the input voltage is 2.5 V and 40 V, the output voltage is 2.35 V and 2.42 V respectively. Therefore, the Line regulation of the proposed LDO can be calculated with a value of 1.86 mV/V. And it is confirmed that the input supply range meets the requirement of wide input voltage from 2.5 V to 40 V, making it suitable for new energy vehicle applications. Furthermore, the output can be established within 30μs, which is determined by the settling time of the charge pump.

Figure 13 depicts the measured transient response of the proposed LDO under different load conditions, (a) I_{load} from 3 mA to 10 mA at V_{IN} = 2.5 V, and (b) I_{load} from 3 mA to 60 mA at V_{IN} = 5 V. The measurement results demonstrate that the undershoot voltage is 52 mV and 32 mV, respectively, when the load current varies from 3 mA to 10 mA at V_{IN} = 2.5 V. Under heavy load and light load conditions, the output voltage is nearly equal, and its value is 2.353 V. When V_{IN} = 5 V, and the load current varies from 3 mA to 60 mA, the output voltage is 2.388 V under light load and 2.288 V under heavy load, so the load regulation of 1.75 mV/mA is achieved.



(a) (b)

Figure 13 The measured transient response of the proposed regulator with (a)I_{load} from 3 mA to 10 mA, V_{IN} = 2.5 V amd (b)I_{load} from 3 mA to 60 mA, V_{IN} = 5 V



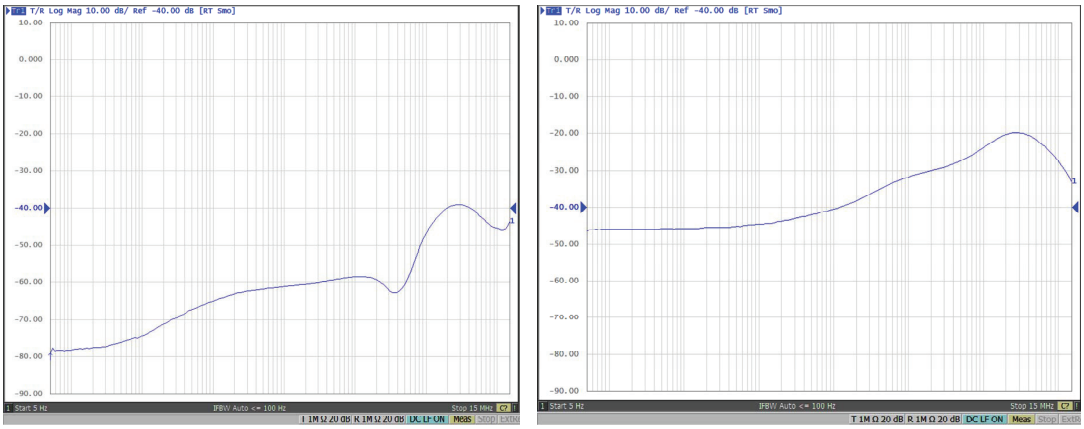
(a) (b)

Figure 14 The measured transient response of the proposed regulator with (a) V_{pulse} from 4.5 V to 5.5V, I_{load} = 3 mA and (b) V_{pulse} from 9 V to 10 V, I_{load} = 60 mA

Figure 14 depicts the measured transient response of the proposed regulator under varying input voltage conditions, with (a) V_{pulse} ranging from 4.5 V to 5.5 V at a constant load current of 3 mA and (b) V_{pulse} ranging from 9 V to 10 V at a constant load current of 60 mA. The measurement results demonstrate that the maximum output voltage spike is less than 60 mV, regardless of whether V_{IN} varies from 4.5 V to 5.5 V or 9 V to 10 V, at both 3 mA and 60 mA load conditions. This indicates that the proposed LDO has good dynamic response capability.

The measured PSR is shown in Figure 15. Under the conditions of V_{IN} = 12 V, I_{load} = 3 mA and 60 mA, the PSR is characterized using a Network Analyzer in the range of 5 Hz to 15 MHz. It can be seen that when I_{load} = 3 mA, PSR is better than -75 dB at 5 Hz and better than -40 dB at 15 MHz. And when I_{load} = 60 mA, PSR is better than -45 dB at 5 Hz and better than -30 dB at 15 MHz. It is worth noting that PSR is better than -20 dB at full frequency.

Table 3 summarizes the performance of the proposed regulator and provides a comparison with other state-of-the-art works, focusing on the wide input voltage range and PSR. Compared with other works, the load capacitor of the proposed LDO is smaller, only 1nF. The results indicate that the proposed LDO has advantages over a wide input voltage range with a PSR of better than -20dB at full frequency, line regulation of 1.86 mV/V, and load regulation of 1.75 mV/mA. In addition, the area also appears to be smaller than that of the other LDOs.



(a) **(b)**

Figure 15 The measured PSR waveforms from 5Hz to 15 MHz,(a)I_{load} = 3 mA,(b)I_{load} = 60 mA

Table 3 Performance comparison between the proposed and some previously reported regulators.

Parameter	14	17	21	23	24	This work
Technology(um)	0.5	0.18	0.6	0.18	0.18	0.18
Vin(V)	2.3-5.5	1.8	4-40	5-12	>69	2.5-40
Vout(V)	1.2-5.4	1.2	2.5-5	3.97	66.7	2.35
Vdrop(mV)	>200	>200	>200	>200	>200	150
Max.I_{load}(mA)	150	10	30	50	100	60
C_L(uF)	NA	NA	1	2.2	0.006	0.001
Line regulation(mV/V)	2.88	10	NA	NA	90	1.86
load regulation (mV/mA)	0.05	4	NA	0.34	1.7	1.75
PSR(dB)	NA	$-41_{@1MHz}$	NA	$-40_{@50KHz}$	NA	$<-20_{@5Hz-15MHz}$
Area(mm^2)	0.0279	0.079	0.3	0.184	0.15	0.09

5 | CONCLUSION

In this study, we have introduced a novel architecture for an LDO that incorporates a closed-loop charge pump and cascode NMOS pass transistors to improve PSR. The charge pump unit employs a new structure to mitigate the impact of body effects, and the voltage reference is supplied by the output voltage of the LDO. The proposed LDO has an input voltage range of 2.5 V to 40 V and can provide up to 60 mA current drive capability. To enhance the reliability of the LDO in the complex electromagnetic environment of automotive applications, we have proposed a power-down protection circuit that has been verified to be effective. The measured line and load regulations have been significantly improved to 1.86 mV/V and 1.75 mV/mA, respectively. Furthermore, we have obtained a measured PSR performance of −65 dB and −45 dB under light loads at 1.5 kHz and 15 MHz, respectively. The measured results confirm that a PSR performance of −20 dB under heavy loads has been achieved at full frequency.

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Conflict of interest

The authors declare no potential conflict of interests.

Data Availability

The datasets supporting the conclusions of this article are included within the article.

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